

AMENDMENTS TO THE CLAIMS

Please **CANCEL** claims 25 and 26 without prejudice or disclaimer.

Please **AMEND** claims 1-3, 5 and 7-24 as shown below.

The following is a complete list of all claims in this application.

1. (Currently Amended) A liquid crystal display (LCD), comprising:
a plurality of gate lines;
a plurality of data lines intersecting the gate lines;
~~a timing controller receiving image signals and synchronization signals, and generating control signals;~~
a data driver generating data voltages for the data lines; and
~~a gate driver sequentially applying generating a stepped-wave pattern gate signals voltage to a plurality of for the gate lines, the each stepped-wave pattern gate voltage signal including:~~
~~a reset interval for converting a grayscale level of a first liquid crystal capacitor a pixel corresponding connected to a subsequent gate line through a first thin film transistor to a first an extreme grayscale level[[,]]; a gate-on interval following the reset interval;[[,]] and an overshoot-interval following the gate-on interval and having the same polarity of with a data voltage applied to the pixel; and~~

~~a data driver for applying the data voltage to the second liquid crystal capacitor of the liquid crystal panel according to the control signals of the timing controller.~~

2. (Currently Amended) The liquid crystal display LCD of claim 1, wherein the first extreme grayscale level is a black grayscale level ~~when~~ in a normally white mode.

3. (Currently Amended) The liquid crystal display LCD of claim 1, wherein the first extreme grayscale level is a white grayscale level ~~when~~ in a normally black mode.

4. (Cancelled)

5. (Currently Amended) A drive method for a liquid crystal display (LCD), comprising:

sequentially applying a stepped-wave pattern gate ~~voltage~~ signals to the gate lines, ~~the each~~ stepped-wave pattern gate ~~voltage~~ including signal comprising:

~~a reset interval for converting a grayscale level of a first liquid crystal capacitor connected a pixel corresponding to a subsequent gate line through a first thin film transistor to a first an extreme grayscale level,~~

a gate-on interval following the reset interval, and

~~an overshoot interval following the gate-on interval and having the same polarity of with a data voltage applied to the pixel; and~~

applying the data voltage to the pixel second liquid crystal capacitor of the liquid crystal panel.

6. (Cancelled)

7. (Currently Amended) The method of claim 5, wherein the gate voltage signal in the reset interval is identical in has the same polarity to a polarity of with the gate voltage signal in the overshoot interval.

8. (Currently Amended) The method of claim 5, wherein the gate voltage signal in the reset interval is opposite in has a different polarity to a polarity of from the gate voltage signal in the overshoot interval.

9. (Currently Amended) The method of claim 5, wherein a voltage level of the gate voltage signal in the overshoot interval is +3V to +10V relative to a gate-off voltage.

10. (Currently Amended) The method of claim 5, wherein the overshoot interval starts at a point where when the gate-on interval ends, and converts to a gate-off voltage at a position where when the gate-on interval doubles.

11. (Currently Amended) The method of claim 5, wherein the first extreme grayscale level is a white grayscale level when in a normally black mode.

12. (Currently Amended) The method of claim 5, wherein the ~~first~~ extreme grayscale level is a black grayscale level ~~when~~ in a normally white mode.

13. (Currently Amended) The method of claim 5, wherein a voltage level of the gate voltage signal in the reset interval is +3V to +10V relative to a gate-off voltage.

14. (Currently Amended) The method of claim 5, wherein ~~a starting point of~~ the reset interval is starts within about 0.5 μ s to about 5 μ s from ~~a starting point of~~ after the gate-on interval starts.

15. (Currently Amended) A liquid crystal display (LCD), comprising:
a gate driver generating a gate signal;
a data driver generating a first data voltage and a second data voltage;
a first gate line transmitting the gate signal;
a second gate line neighboring the first gate line and transmitting the gate signal;
a data line ~~for intersecting the first and second gate lines and transmitting the first data signal and the second data signal~~ a first data voltage and a second data voltage;
a first switching element connected to the first gate line and the data line and selectively transmitting the first data voltage to a first pixel;
a second switching element connected to the second gate line and the data line and selectively transmitting the second data voltage to a second pixel;
a first liquid crystal capacitor ~~connected to capacitance formed at the first switching element pixel;~~

a second liquid crystal capacitor connected to capacitance formed at the second switching element pixel;

a storage capacitor connected capacitance formed between the second liquid crystal capacitor capacitance and the first gate line[;]]

~~a data driver applying the first and the second data voltages to the data line; and a gate driver sequentially applying the gate signal to the first and the second gate lines,~~

wherein the gate signal applied to the first gate line has a first interval having a first voltage converting a grayscale level of the second pixel to an extreme grayscale level, a second interval following the first interval and having a second voltage, a third interval following the second interval and having a third voltage and a fourth interval following the third interval and having a fourth voltage first, second, third, and fourth voltages during sequentially arranged first, second, third, and fourth time intervals, respectively.

16. (Currently Amended) The liquid crystal display LCD of claim 15, wherein the first switching element and the second switching element turn is turned on by the second voltage and turn turned off by the fourth voltage.

17. (Currently Amended) The liquid crystal display LCD of claim 16, further comprising a common line providing a common voltage for the first liquid crystal capacitance and the second liquid crystal capacitance,

wherein the first liquid crystal and the second liquid crystal capacitor are supplied with a common voltage, the third voltage of the gate signal applied to the first gate line is higher greater than the fourth voltage when the first data voltage is higher than the common voltage, and the third voltage of the gate signal applied to the first gate line is lower than the fourth voltage when the first data voltage is lower less than the common voltage.

18. (Currently Amended) The ~~liquid crystal display LCD~~ of claim 17, wherein both the first and the third voltages are higher or lower than the fourth voltage.

19. (Currently Amended) The ~~liquid crystal display LCD~~ of claim 18, wherein the liquid crystal display operates in a normally white mode.

20. (Currently Amended) The ~~liquid crystal display LCD~~ of claim 17, wherein one of the first and the third voltages is higher greater than the fourth voltage and the other of the first and the third voltages is lower less than the fourth voltage.

21. (Currently Amended) The ~~liquid crystal display LCD~~ of claim 20, wherein the liquid crystal display operates in a normally black mode.

22. (Currently Amended) The ~~liquid crystal display LCD~~ of claim 16, wherein both the first and the third voltages are higher or lower than the fourth voltage.

23. (Currently Amended) The liquid crystal display LCD of claim 22, wherein a level of the third voltage has a value is between levels the first voltage and the fourth voltage.

24. (Currently Amended) The liquid crystal display LCD of claim 16, wherein one of the first and the third voltages is higher greater than the fourth voltage and the other ~~of the first and the third voltages~~ is lower less than the fourth voltage.

25-26. (Cancelled)